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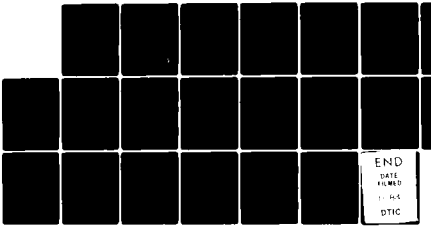

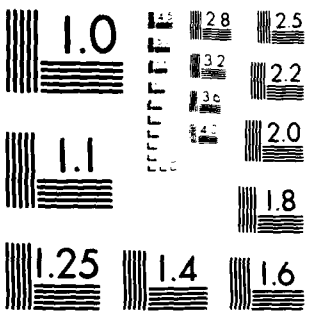

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Influence of the atomic roughness at the Si-Si-O_2 Interface

FINAL TECHNICAL REPORT

by

M. Henzler and P.O. Hahn

Institut für Festkörperphysik
Universität Hannover, W-Germany

September 82

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Si/SiO_2 interface - Mobility in inversion layers - Roughness determination - MOS-devices

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Special MOS-FET's have been prepared to check a correlation between the atomic roughness at the Si/SiO_2 interface (as determined by the novel technique of spot profile analysis in the LEED pattern, SPA-LEED) and the electronic mobility in the MOS-device. The transistors have been tested in the temperature range

from room temperature down to liquid helium (4 K). Four different sets of transistors with different roughness have been prepared. The roughness has been determinated at large areas with gate oxide on the same chip (without transistor structures however). Premilinary measurements of mobility show the predicted correlation between roughness and mobility.

Summary

Special MOS-FET's have been prepared to check a correlation between the atomic roughness at the Si/SiO_2 interface (as determined by the novel technique of spot profile analysis in the LEED pattern, SPA-LEED) and the electronic mobility in the MOS-devices. The transistors have been tested in the temperature range from room temperature down to liquid helium (4 K). Four different sets of transistors with different roughness have been prepared. The roughness has been determinated at large areas with gate oxide on the same chip (without transistor structures however). Premilinary measurements of mobility show the predicted correlation between roughness and mobility.

Preliminary

Keywords: Si/SiO_2 interface
Mobility in inversion layers
Roughness determination
MOS-devices

0. Publications and Presentations

1. P.O. Hahn and M. Henzler:
   Influence of Oxidation parameters on Atomic Roughness at the Si-SiO_2 Interface in "Insulating Films on Semiconductors", Ed.M. Schulz and G. Pensl in Springer Series in Electrophysics 7, Springer Verlag, Berlin-Heidelberg-New York, 1981

2. P.O. Hahn and M. Henzler, J. Appl. Phys. 52, 1981, 4122

3. M. Henzler, Appl. Surf. Sci 11/12, 1982, 450

4. Talks at Conferences and Special Seminars:

   27.4.81 P.O. Hahn at INFOS 81 in Erlangen

   29.4.81 M. Henzler at WEK-Seminar in Bad Honnef (invited talk)

   10.6.81 M. Henzler at ICSFS-2 in College Park Maryland (invited talk)

   1.6.81 M. Henzler at University of Wisconsin, Maryland

   3.6.81 M. Henzler at University of Ill., Urbana, Ill.

   5.6.81 M. Henzler at Bell Labs, Murray Hill, N.J.

   12.6.81 M. Henzler at US Army El. and Dv. Lab., Fort Monmouth, N.J.

   16.6.81 M. Henzler at IBM Research, Yorktown Heights, N.Y.

   17.6.81 M. Henzler at Exxon Research, Linden, N.J.

   9.11.81 M. Henzler at Universität München

   11.11.81 M. Henzler at Technische Universität München

   17.12.81 M. Henzler at Conference of the Italian National Research Council in Modena, Italy (invited talk)

   1.4.82 P.O. Hahn at 46. Physikertagung Münster 1982

   14.6.82 P.O. Hahn at Physical Electronics Conference in Atlanta, N.J. - This paper has got the "Nottingham Prize" for the best theses presented at the Conference

   30.8.82 M. Henzler at 2nd IUPAP/UNESCO-Symposion on Semiconductor Surfaces and Interfaces in Trieste, Italy (invited talk)

Influence of atomic roughness at the Si-Si O_2 interface on mobility in silicon inversion layers
Performance of MOS-transistors with well defined roughness at the interface (final report).

by

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I. Introduction

In the first two reports we have shown, that the oxidation parameters determine the atomic roughness at the Si/SiO_2 interface. We have developed a new method enabling us for measuring the atomic roughness on an atomic scale at the interface. Now it is for the first time possible to produce devices with a well defined roughness at the interface for a direct comparison of structural and electronic properties of devices.

The carrier mobility in MOS inversion-layers has been measured at low temperatures in the last twenty years by several groups (Cheng and Sullivan (1), Yagi (2), Kawaji (3), Kawaguchi (4), N.St.J. Murphy, F.Berz and I.Flinn (5,6) and P. Balk (7). The results have been explained with different scattering processes. The main results are:
For low carrier concentrations the coulomb scattering is the dominant process. The coulomb centres are screend (1,2) by the charge carriers and the mobility increases with increasing carrier concentration. For medium carrier concentration ($\sim 10^{12}$ cm^{-2}) neutral impurities are important for the scattering process (8). For high carrier concentrations the decrease of mobility is explained with the scattering at the atomic roughness of the interface since the channel becomes smaller with increasing gate voltage. Theoretical calculations of J.R. Schriefer (9), F. Stern and W.E. Howard (10) and Cheng (11) support qualitatively and quantitatively the influence of the atomic roughness on carrier mobility.

Up to now the existence of steps at the interface could be shown with TEM-measurements (12, 13) without quantitative determination, however. The aim of this work is now to show directly and quantitatively the correlation of the atomic roughness on an atomic scale with the mobility in MOS-inversion layers.

For that purpose special MOS-transistor chips were designed. After gate-oxidation every high temperature step had to be avoided to have a wide range of interface roughness. One third of the chip was prepared in such a way, that this region showed only the gate-oxide. Probes were cut from this regions for measuring the roughness with the novel SPA-LEED method as described in the previous report. Now we report the performing of MOS-devices with a well defined roughness and showed that they were working sufficiently.

II. Experimental

1. Production of the MOS-structures

To show the influence of the atomic roughness on the channel-mobility MOS-transistors with known roughness had to be built. In the previous reports the oxidation parameter are given to obtain a small or large roughness at the interface. Each handling in a high temperature atmosphere changes the roughness. Therefore every high temperature step after the gate-oxidation had to be avoided. For measuring Hall mobility besides source and drain two additional Hall-contacts are required, p-channel transistors were produced on n-substrates to avoid problems with a zero voltage inversion layer. Moreover Shipley-lac has been used beeing a positive lac technology. The UV exposed places were etched away. For simplicity the concept was realized with only three masks:

Mask 1 (see fig. 1): This mask is used for etching those regions in the oxide, which should become p-type silicon by ion-implantation.
Mask 2 (see fig. 2): After the gate-oxidation this mask is used to open windows for the aluminum contacts to p-type silicon.
Mask 3 (see fig. 3): After aluminum deposition this mask is used to etch away the metal between the contacts.

About four hundred transistors were built per chip (see fig.4). One third of the chips was covered always during processing, that it only shows the gate-oxide identical to that of the transistors. From this reference material samples for the LEED-measurements were prepared and the atomic roughness of the transistors R 1 - R 4 accordingly to those reference samples were measured later with the earlier described LEED-experiments. In this way, we received transistors with an exactly measured roughness.

In the following, the technology to built a MOS-transistor is described and summarized in the figure (5):

a) Preparation of the chips

It was started with n-type (5 - 10 Ω cm), etch-polished, "3" in diameter and (111) oriented silicon chips. Those chips were reduced by etching to a diameter of 25 mm needed for the technology. Before each step in processing the chips cleaned according to the following standard cleanig process:

1. Dipping in concentrated nitric acid for ten minutes in a quartz cup
2. Rinsing in bidistilled H_2O (2x)
3. Boiling in nitric acid (60 %) (p.a.) for 30 minutes in a quartz cup
4. Boiling in bidistilled H_2O (30 minutes)
5. Rinsing in bistilled H_2O (3x)

Now the chips were dried.

b) Ion-implantation

To receive p-type regions of high doping level ion-implantation technology was used. As a mask for implantation we used a thermally grown thick silicon-oxide layer of about 7000 Å (see fig. 5, step a). After implantation the whole oxide has to be removed by etching to grow then the gate-oxide, but an exact adjustment of the second mask then is impossible.

Therefore an oxidation only for adjustment is necessary. The chips were oxidized in such a way, that after etching of the windows (source, drain, Hall-contacts) an oxide of 900 Å is formed. This oxide consumed about 450 Å silicon. While the growth of the thick oxide (7000 Å) is negligible, we receive after etching of the oxide regions (source, drain), which were down to a level of about 450 Å. This step could be seen unter the microscope and an adjunstment was now possible.

In a first attempt the chips were doped by thermal diffusion. But measurements at T = 4.2 K showed, that the doping concentration was too small, so that all carriers were frozen out at all temperatures below T = 50 K. In consequence the very high resistivity of the contacts prevented successful measurements of mobility.
Now the technology of the ion-implantation was used, where the concentration of ions is exactly choosable. As a dopant boron was choosen. The results of F.J. Morin and J.P. Maita (14) showed, that silicon is degenerate at a boron concentration of about $1,5 \cdot 10^{19}$ cm^{-3}. Therefore this concentration is suffizient.Further it had to be considered, that the boron ions had to penetrate the oxide. After the implantation the whole oxide will be removed by etching and the following gate oxidation of about 1200 Å oxide will need 600 Å silicon. These parameters determine the depth of the maximum of the boron concentration to about 1500 Å, requiring an energy of the ions of about 60 keV (15,16). The implantation was performed in the "Fraunhofer Institut für Angewandte Festkörperphysik", Freiburg by Dr. Axmann. The expected profile of the boron concentration is shown in the figure (6). The implantation parameters were: B^+-ions; D = 10^{15} cm^{-2}; E = 60 keV; 30 minutes. The maximum is at Rp = 1403 Å with a Δ Rp = 556 Å. After the implantation all samples were annealed at 900° C for 30 minutes (16) to restore the ideal lattice, which was damaged by the ions.

c) Gate-oxidation and Al-contacting

Now the oxide of all chips was completely etched away. All the chips were subjected to the standard cleaning process. Then the gate-oxide was produced with the following oxidation parameters. The thickness of all four chips was about 1200 Å.

chip	parameter of gate-oxidation
R 1	2 3/4 hours, in dry O_2 at 1000° C
R 2	2 3/4 hours, in dry O_2 at 1000° C and 4 hours annealed in N_2 (1000° C)
R 3	9 minutes, wet at 1000° C
R 4	9 minutes, wet at 1000° C and 4 hours annealed in N_2 (1000° C)

After the gate-oxidation all chips were evaporated with cleaned pure aluminium(9, 96 %) in a diffusion pumping system. Before aluminium depositing all chips were dip etched in buffered HF to remove the native oxide. Then about 200 nm Å Al was deposited at 2×10^{-15} torr. Now the third mask-step was applied. After etching the aluminium in 80 ml H_3PO_4 + 4 ml HNO_3 (65 %) + 16 ml H_2O and annealing the chips at 540° C in N_2-atmosphere for ten minutes complete MOS-fets as shown in fig. (3) and (7) were obtained.

d) Testing, scratching, breaking, alloying and bondig of the transistors

The function of the described transistors were now proved with adjustable tips unter a microscope. Of about 400 transistors per chip worked all right at R 1 67 %, R 2 70 %, R 3 90 % and R 4 72 %. The gates of the defect transistors were marked with a tip for separation.

Now the chips were scratched with a diamond and broken over an edge, so that each piece of silicon contains four well working MOS-fets. Now those silicon pieces were alloyed under N_2-atmosphere at 370° C on a transistor holder. Finally 4 - 5 transistors were bonded unsing gold contacts.

2. Experimental equipment for determining the characteristic curves and charge carrier mobility at low temperatures

All measurements at low temperatures were performed in a cryostat (Firma Leybold), permitting measurements in the temperature range of 1.5 K - 300 K. The cryostat was used as a bath cryostat. An exact description of the equipment is given in ref. 17 and 18. The temperature could be measured both with a vapour pressure thermometer and with a calibrated germanium resistor.
The transistors were mounted on the sample holder at the cryostat and then cooled to the wanted temperature.
The magnetic field was produced with a water cooled electromagnet (Firma Brucker, Typ E 10 D 8). The maximal flux density reached with the magnet was about 0.6 T. Because the polarity could be reversed the Hall-voltage was measured always in the two directions at the maximum magnetic field. In the fig. 7 the electrical circuit is shown. The conductance and Hall-measurements were performed at a homogeneous channel. This is a channel in which the change of the mobility and density along the channel could be neglected. This requirement is fulfilled for a source-drain voltage V_{DS} beeing small in relation to the gate-source voltage V_{gs}. It was measured at V_{SD} = 500 mV.
The homogeneity was often checked by reduction of the source-drain voltage. All electric data of the transistors were measured DC.

III. Results

a) Electric data of the MOS-transistors

The four transistor chips had been handled all in the same way with exception of the gate oxidation. To show the working of the MOS-FET's the caracteristic curves were measured at various temperatures. In fig. (8) and fig. (9) the drain-current as a function of the source-drain voltage for various gate voltage is shown for all four samples at room temperature. They all show the typical curves for MOS-FET's. The curves of R 4 show in comparison to R 3 as well as R 2 to R 1 the higher saturation current.

In fig. (10) and fig. (11) the corresponding measurements are shown for the lowest temperature at T = 4.2 K.

R 4 in comparison to R 3 as well as R 2 to R 1 have again the higher saturation current. Further more the saturation value of the current is drastically increased in reference to room-temperature. Also the break-down voltage is reduced drastically to about 20 V (avalanche break-down) for R 2 and R 4. In contrary to room-temperature the break-down voltage is now higher for R 3 and R 1.

Fig. (12) and (13) show the saturation drain current as a function of the gate-voltage for all samples for T - 4.2 K (fig. 12) and room-temperature (fig. 13). All curves show the expected quadratic current voltage dependance. Remarkable is, that at T = 4.2 K the current of R 3 is higher than R 1 in contrary to room-temperature.

b) Roughness of the four gate-oxidations (R 1 - R 4)

As described in the previous reports the atomic roughness of the gate-oxides were determined by LEED on the reference crystals prepared from the chips. Those measurements were performed on different places on the crystal. The error bars of the calculated step atom density show then their deviations.

The results are summarized in the following table 1.

chip	oxidation parameter	step atom density/%
R 1	dry, at 1000° C, 2 $^{3}/_{4}$ hours +	16,7 ± 4,6
R 2	dry, at 1000° C, 2 $^{3}/_{4}$ hours + 4 hours annealed at 1000° C in N_2	8,1 ± 0,9
R 3	wet, 1000° C, 9 min	21,4 ± 1,8
R 4	wet, 1000° C, 9 min + 4 hours annealed at 1000° C in N_2	9,9 ± 1,7

IV. Discussion

The results (fig. (7) - fig. (13)) have demonstrated, that all transistors show the usual performance down to liquid helium. They are all of the p-channel type. Their gain (0,1 - 0,5 m A/V) is small due to the wide quadratic gate.

At low temperature (4.2 K) all transistors show a higher gain and saturation current, because the phonon scattering is no more present. The gate break-down voltage has a value of about 50 - 60 V, which is comparable with the measurements of Fang and Fowler (19).

V. Conclusion

Now for the first time it will be possible to correlate the mobility with the atomic roughness at the interface directely. Those results will received in the next step performing conductivity and Hall-effect measurements. First preliminary measurements give direct hints to the expected correlation. The results will be reported after completion and evaluation of the measurements.

VI. Acknowledgements

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Figure Captions

Fig. 1 Mask 1 for production of MOS-devices

Fig. 2 Mask 2 " " " "

Fig. 3 Mask 3 " " " "

Fig. 4 Arrangement of transistors (for electrical measurements) and of large area gate oxide (for roughness determination)

Fig. 5 Schematic presentation of device production with 3 masks

Fig. 6 Profile of boron after implantation (calculated)

Fig. 7 Electrical circuit for testing the device and measuring the mobility

Fig. 8 I_D/U_{SD} curves for transistors R 1 and R 2 at 300 K

Fig. 9 same as fig. 8 for R 3 and R 4

Fig. 10 same as fig. 8 at 4 K

Fig. 11 same as fig. 9 at 4 K

Fig. 12 I_D at saturation vs. U_D at 4 K

Fig. 13 same as fig. 12 at 300 K

mask 1

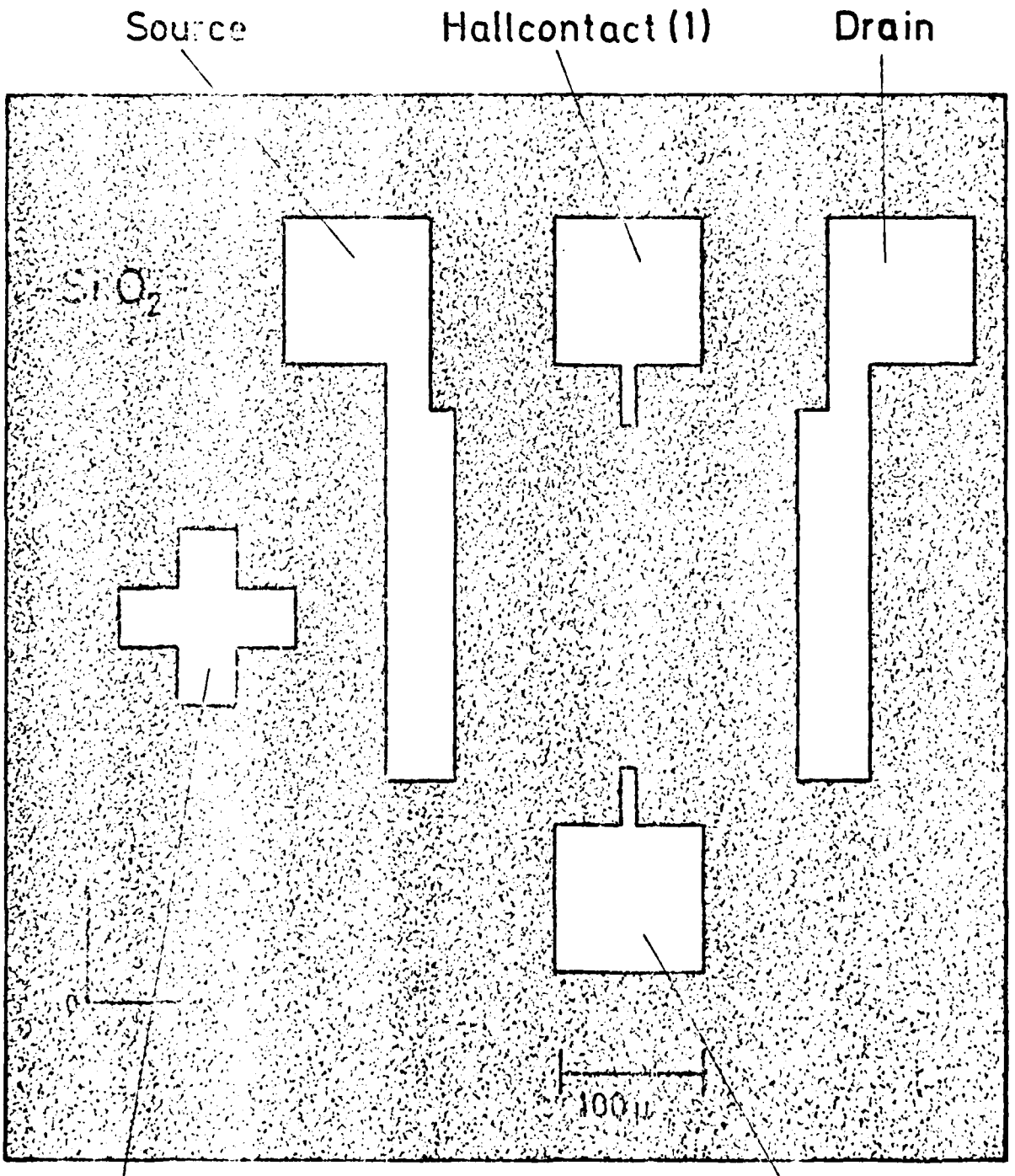

Source
Hallcontact (1)
Drain
SiO_2
100 µ
cross for adjustment
Hallcontact (2)

fig 1

mask 2

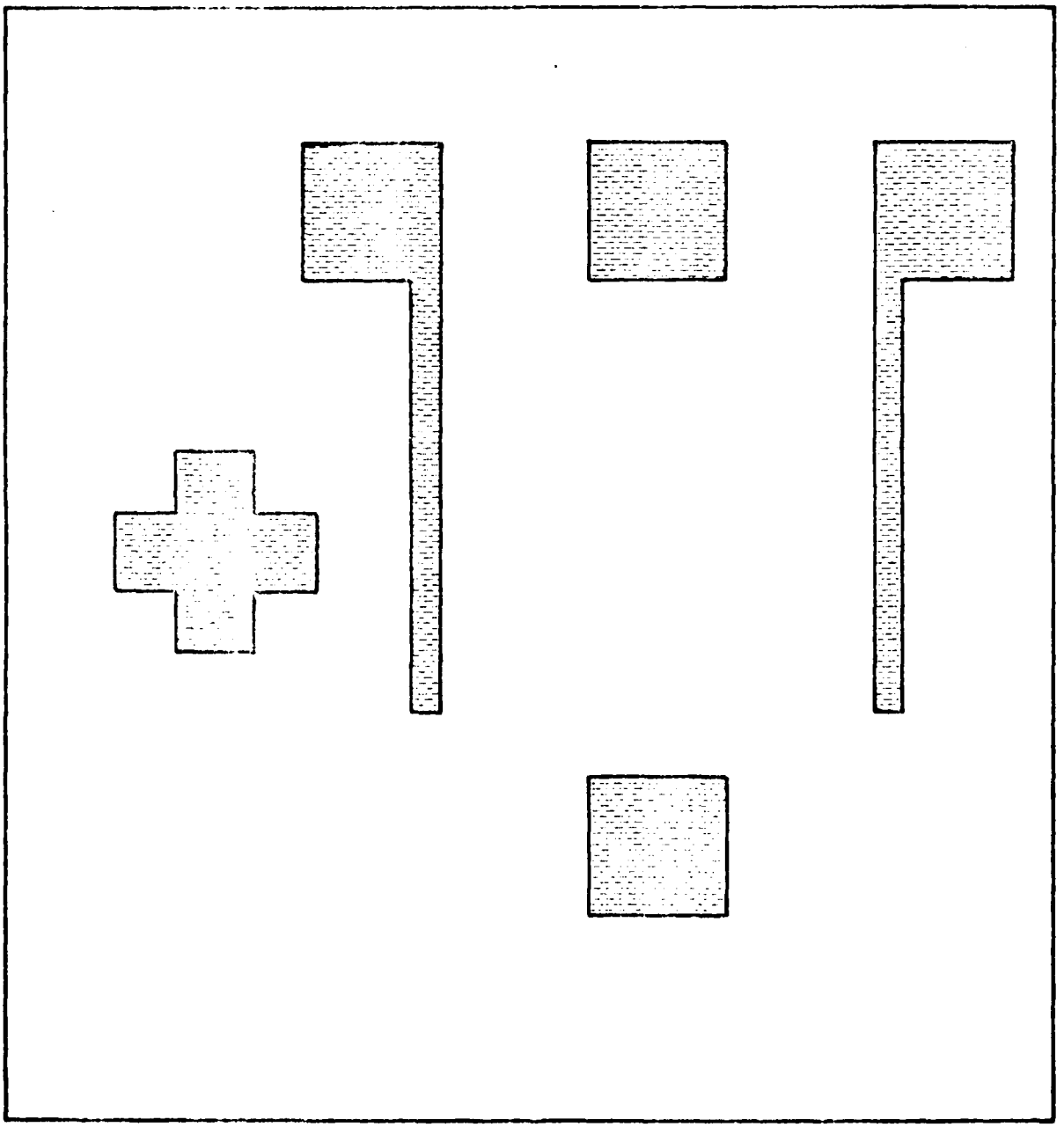


fig 2

mask 3

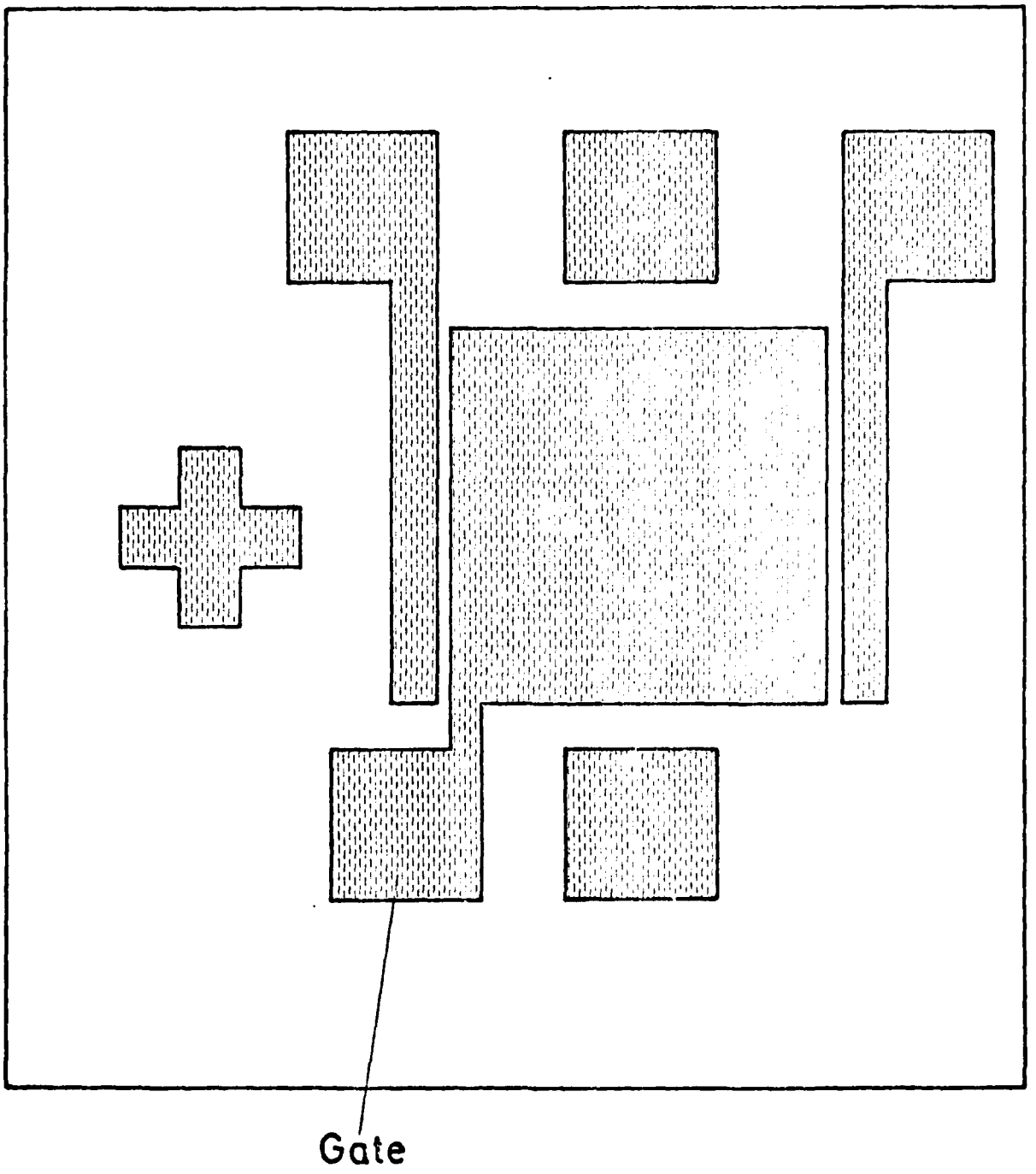


fig 3

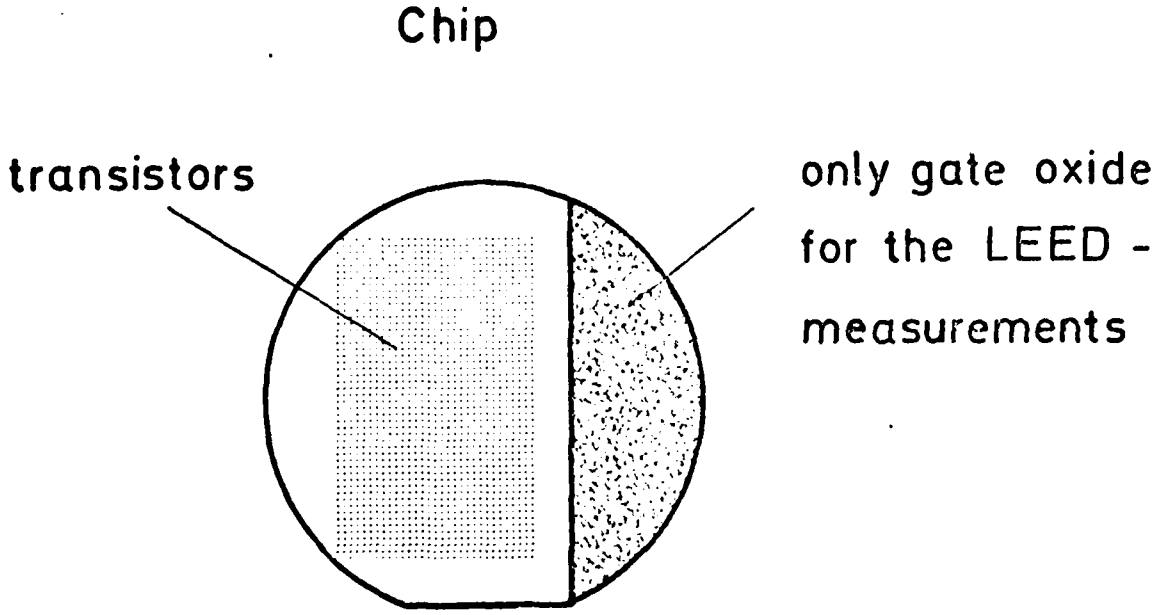
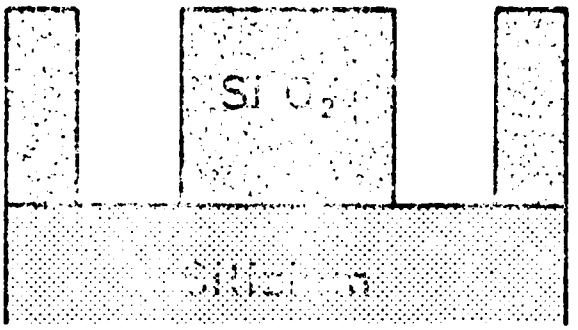

Chip
transistors
only gate oxide
for the LEED -
measurements

fig 4

Device performance (MOS)

a)



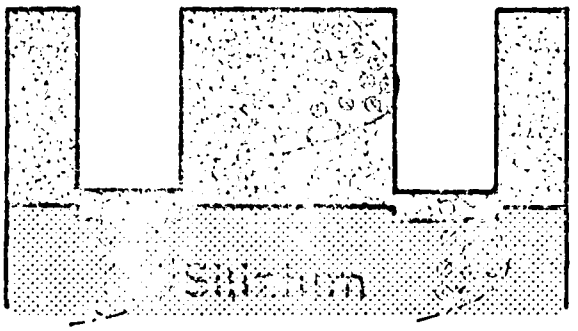
Oxidation (7000 Å)

↓

Etching (1. mask)

baron

b)

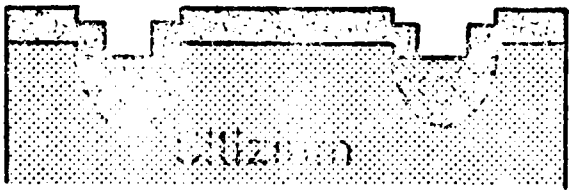


Oxidation for adjustment

↓

ion implantation

c)



Etching (completely)

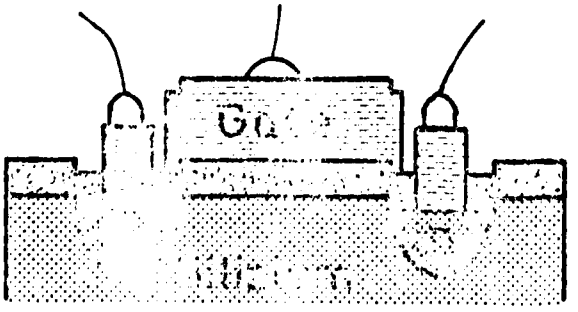
↓

Gate oxidation (1200 Å)

↓

Etching (contacts, 2. mask)

d)



Aluminum - depositing

↓

Alu - etching (3. mask)

↓

bonding

fig 5

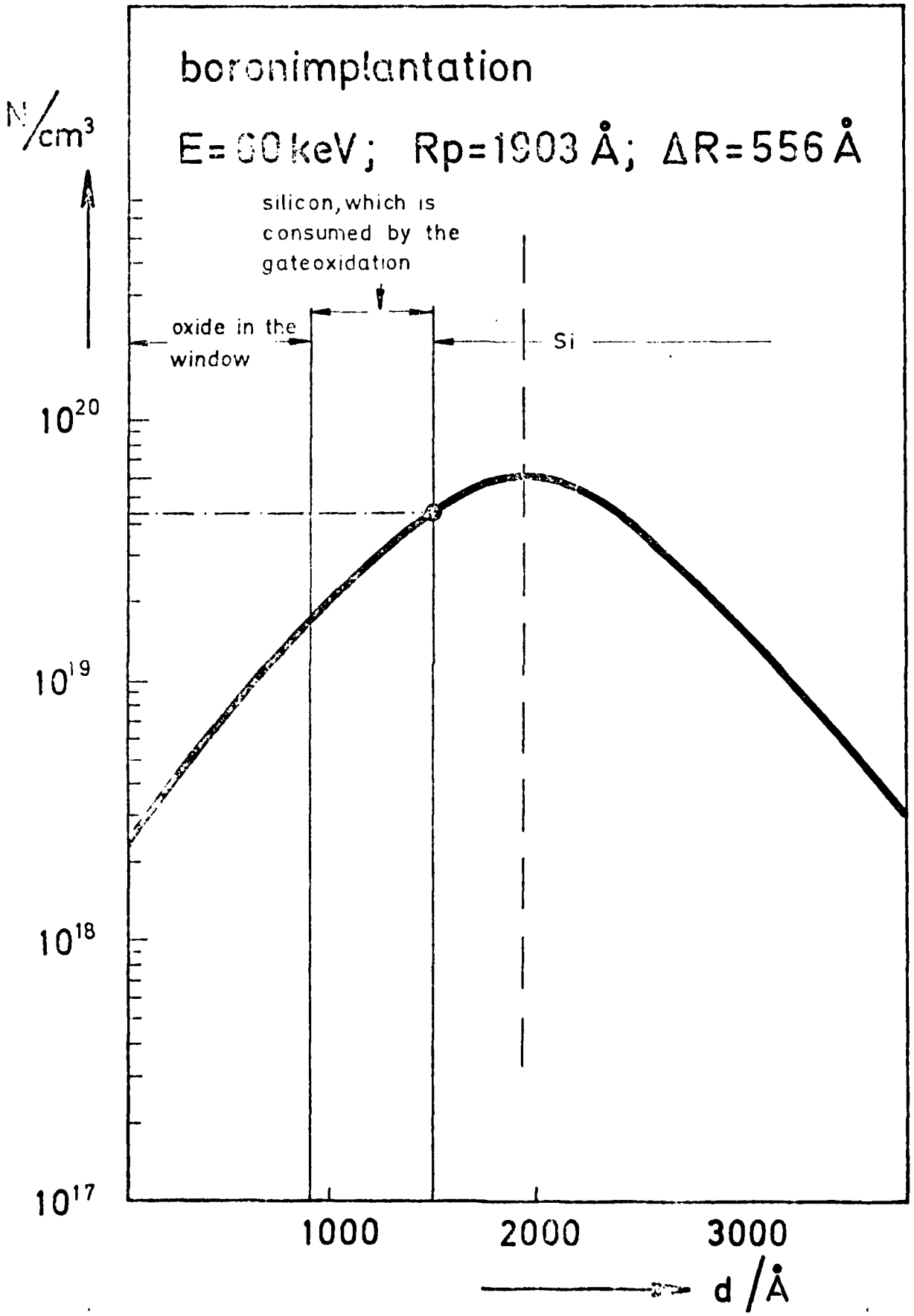
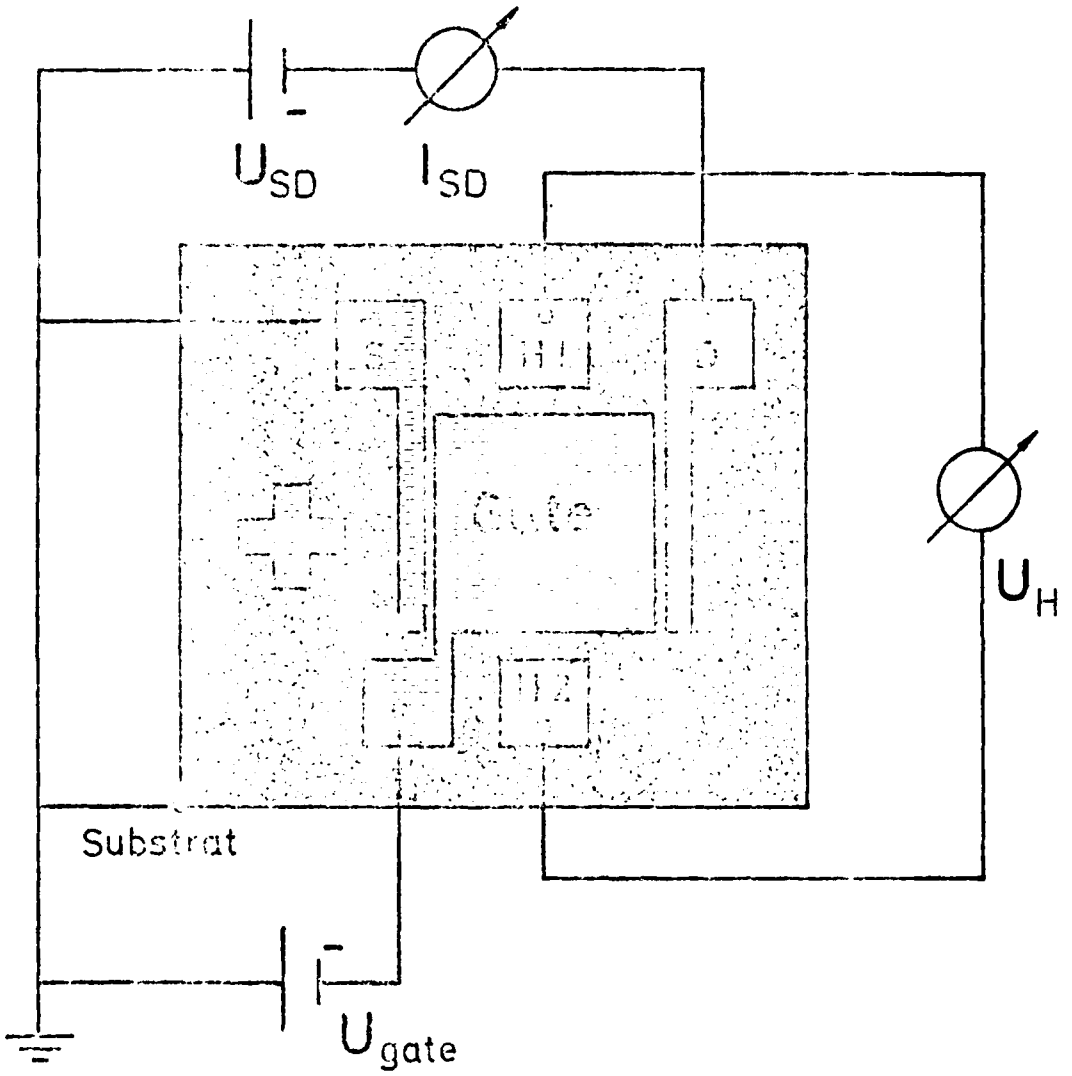

boronimplantation
E=60keV; Rp=1903 Å; ΔR=556 Å
N/cm³
silicon, which is consumed by the gateoxidation
oxide in the window
Si
10²⁰
10¹⁹
10¹⁸
10¹⁷
1000
2000
3000
d /Å

fig 6

halleffect and conductivity measurements



B in both directions 0,6 T

fig 7

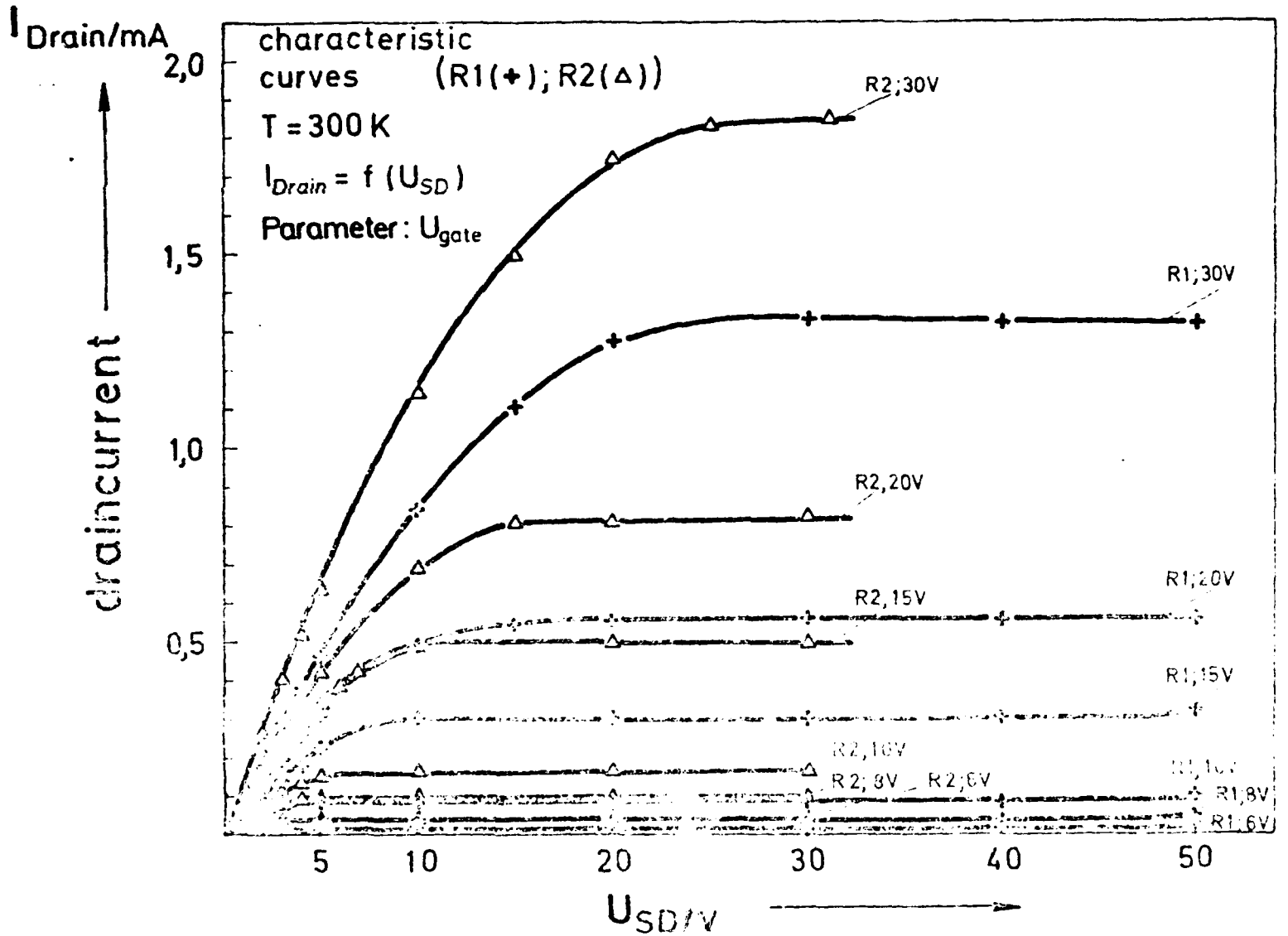

I Drain/mA
characteristic
curves (R1(+); R2(△))
T = 300 K
$I_{Drain} = f(U_{SD})$
Parameter: U_{gate}
draincurrent
2,0
1,5
1,0
0,5
R2;30V
R1;30V
R2,20V
R1;20V
R2,15V
R1;15V
R2;8V
R2;6V
R1,8V
R1,6V
5
10
20
30
40
50
$U_{SD/V}$

fig 8

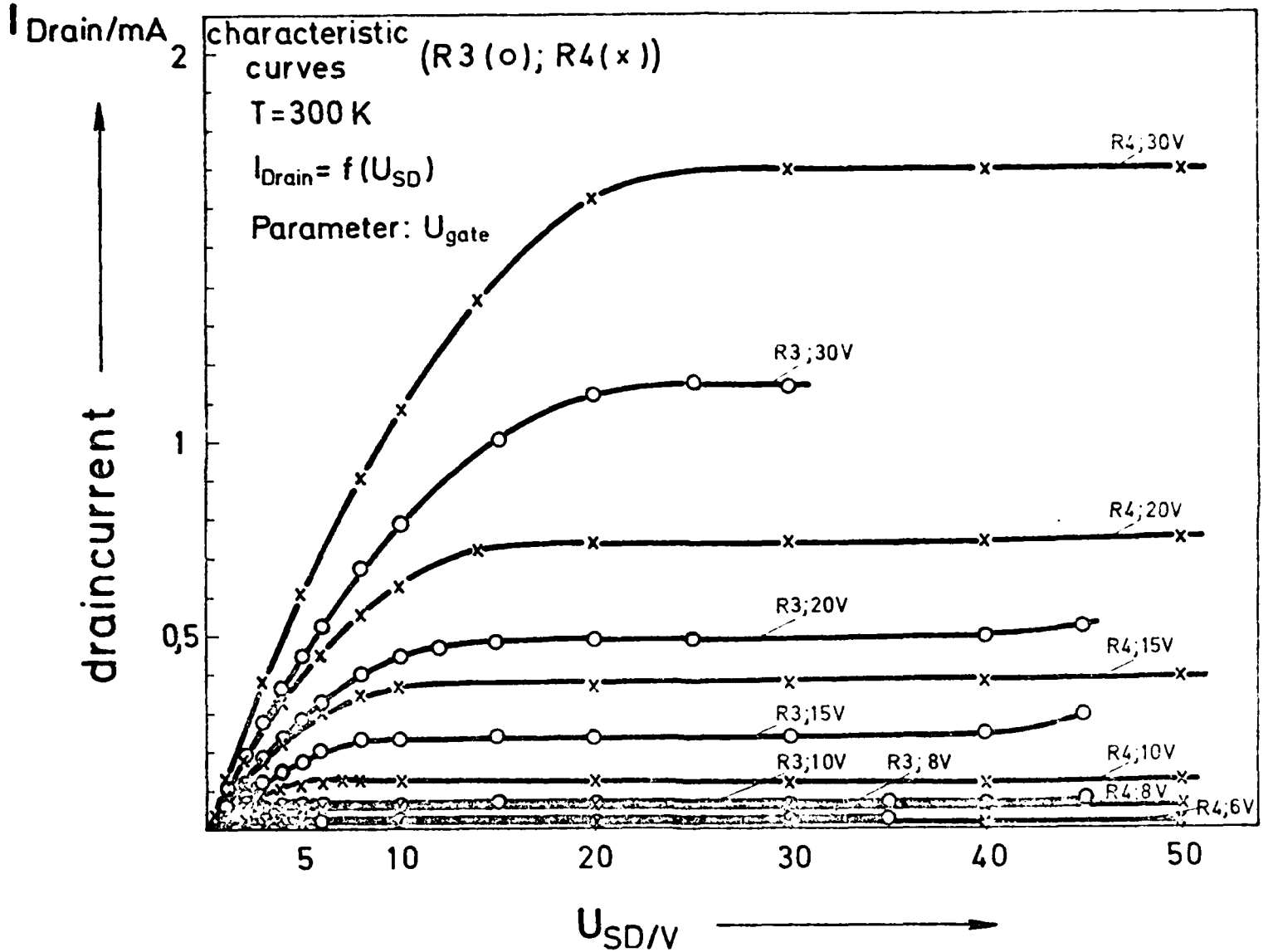

I Drain/mA
2
1
0,5
draincurrent
characteristic curves (R3 (o); R4 (x))
T=300 K
$I_{Drain} = f(U_{SD})$
Parameter: U_{gate}
R4;30V
R3;30V
R4;20V
R3;20V
R4;15V
R3;15V
R3;10V
R3; 8V
R4;10V
R4;8V
R4;6V
5
10
20
30
40
50
$U_{SD/V}$

fig 9

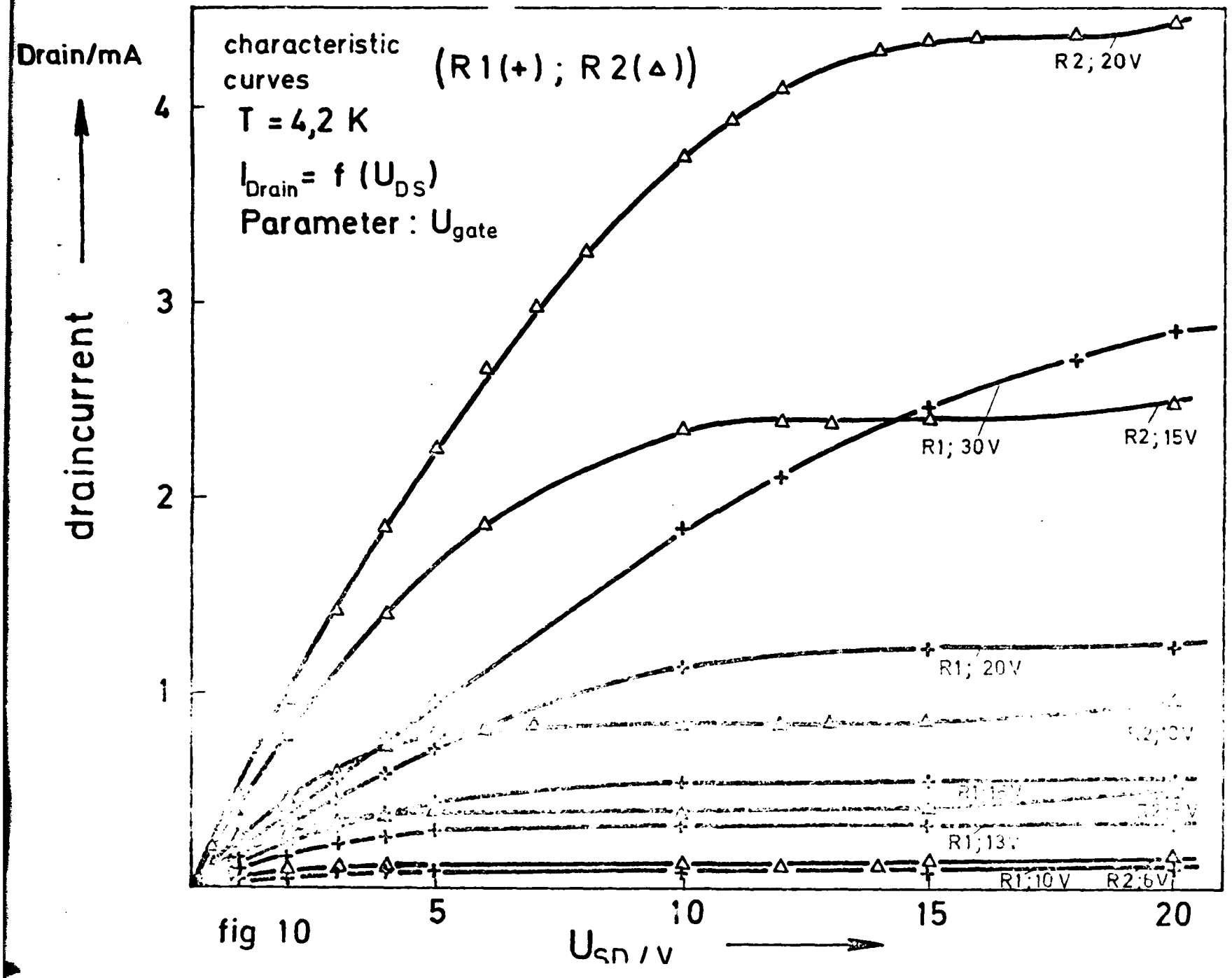

Drain/mA
characteristic curves
(R1(+) ; R2(Δ))
T = 4,2 K
$I_{Drain} = f(U_{DS})$
Parameter : U_{gate}
R2; 20V
R1; 30V
R2; 15V
R1; 20V
R1; 13V
R1; 10V
R2; 6V
4
3
2
1
5
10
15
20
draincurrent
U_{DS} / V

fig 10

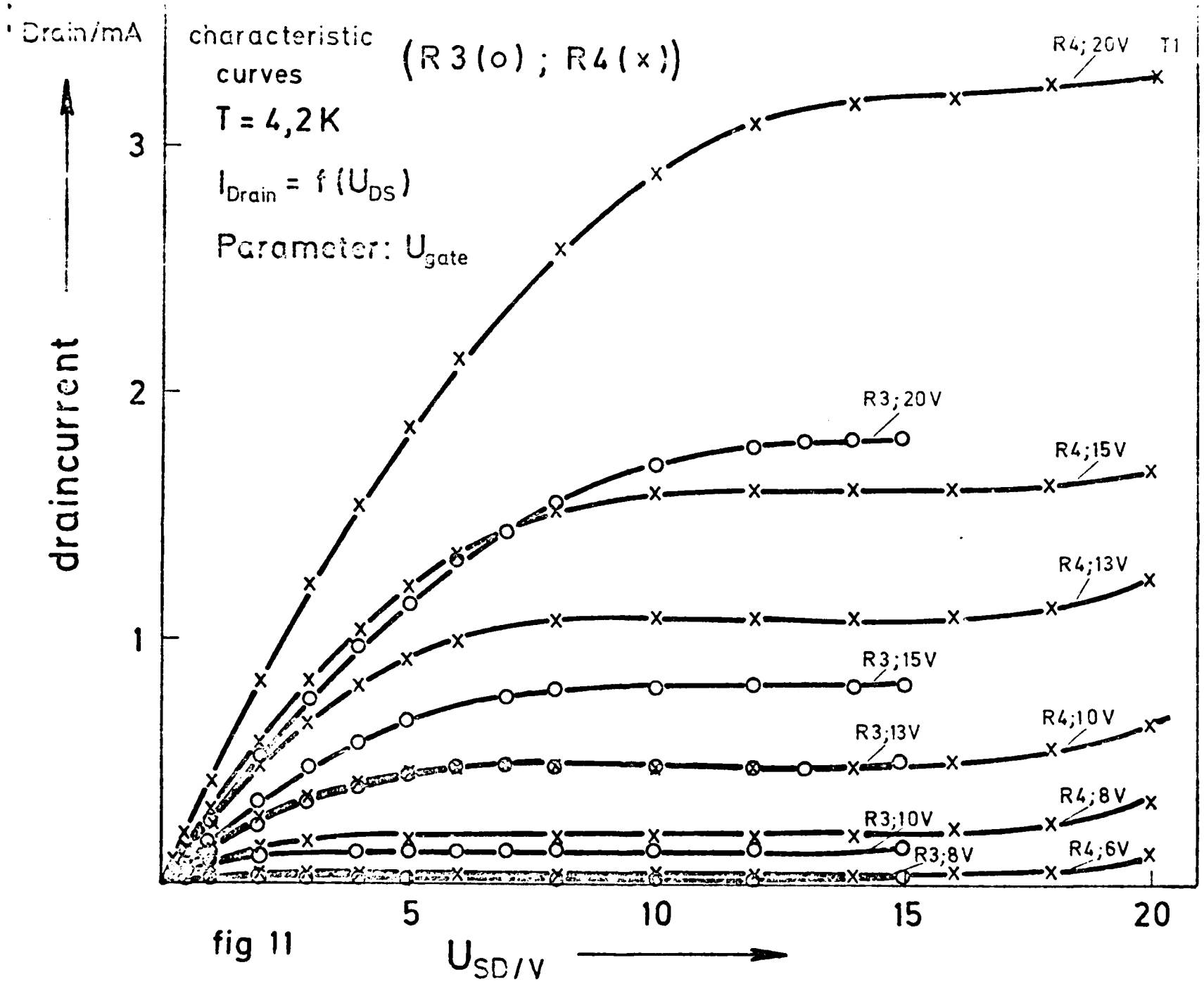

Drain/mA
characteristic curves
(R3(o) ; R4(x))
T = 4,2K
$I_{Drain} = f(U_{DS})$
Parameter: U_{gate}
R4;20V
T1
R3;20V
R4;15V
R4;13V
R3;15V
R4;10V
R3;13V
R4;8V
R3;10V
R3;8V
R4;6V
draincurrent
3
2
1
5
10
15
20
$U_{SD/V}$

fig 11

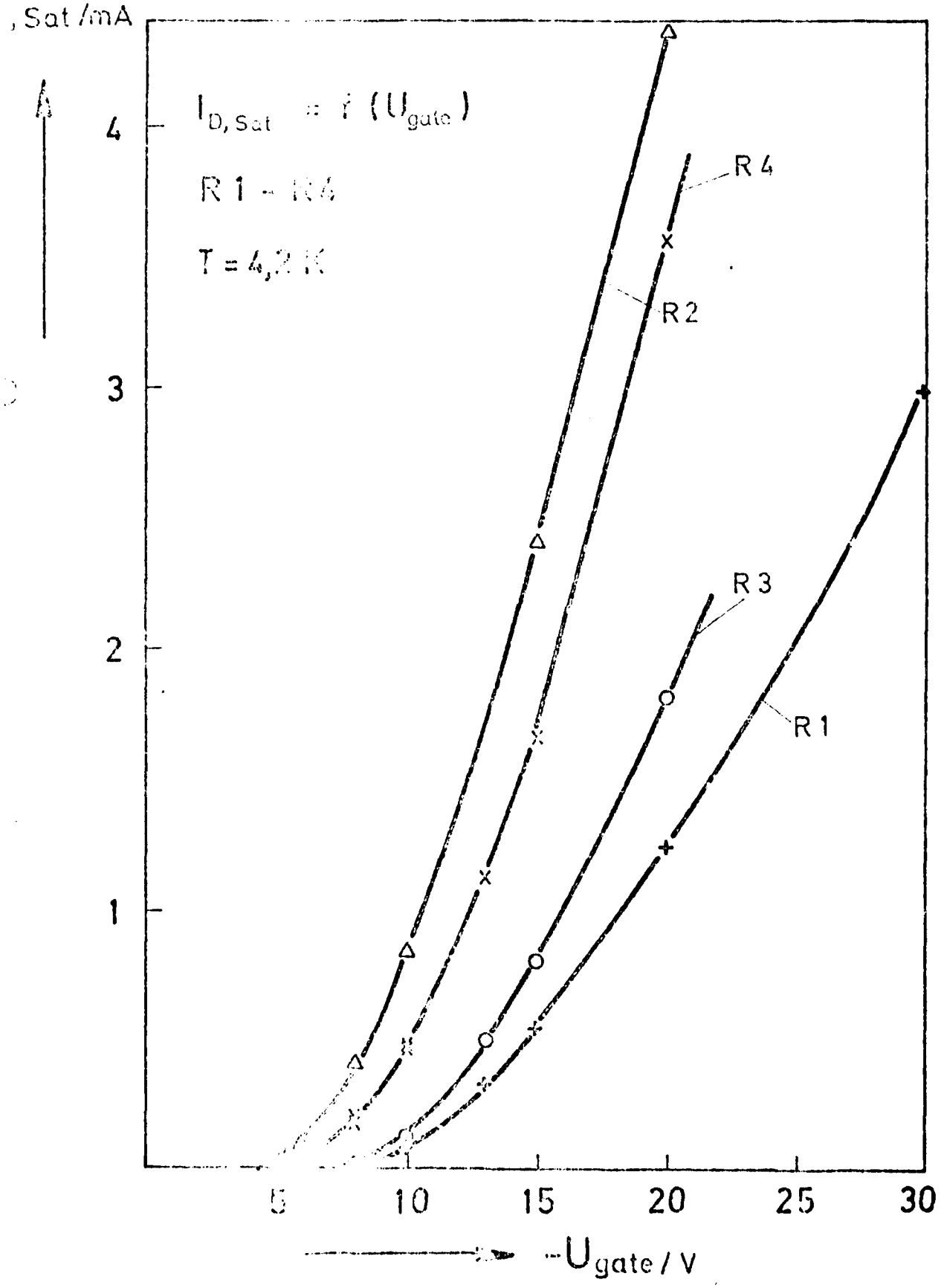

, Sat /mA
$I_{D,Sat} = f(U_{gate})$
R 1 - R 4
T = 4,2 K
R 4
R 2
R 3
R 1
4
3
2
1
5
10
15
20
25
30
$-U_{gate}$ / V

fig 12

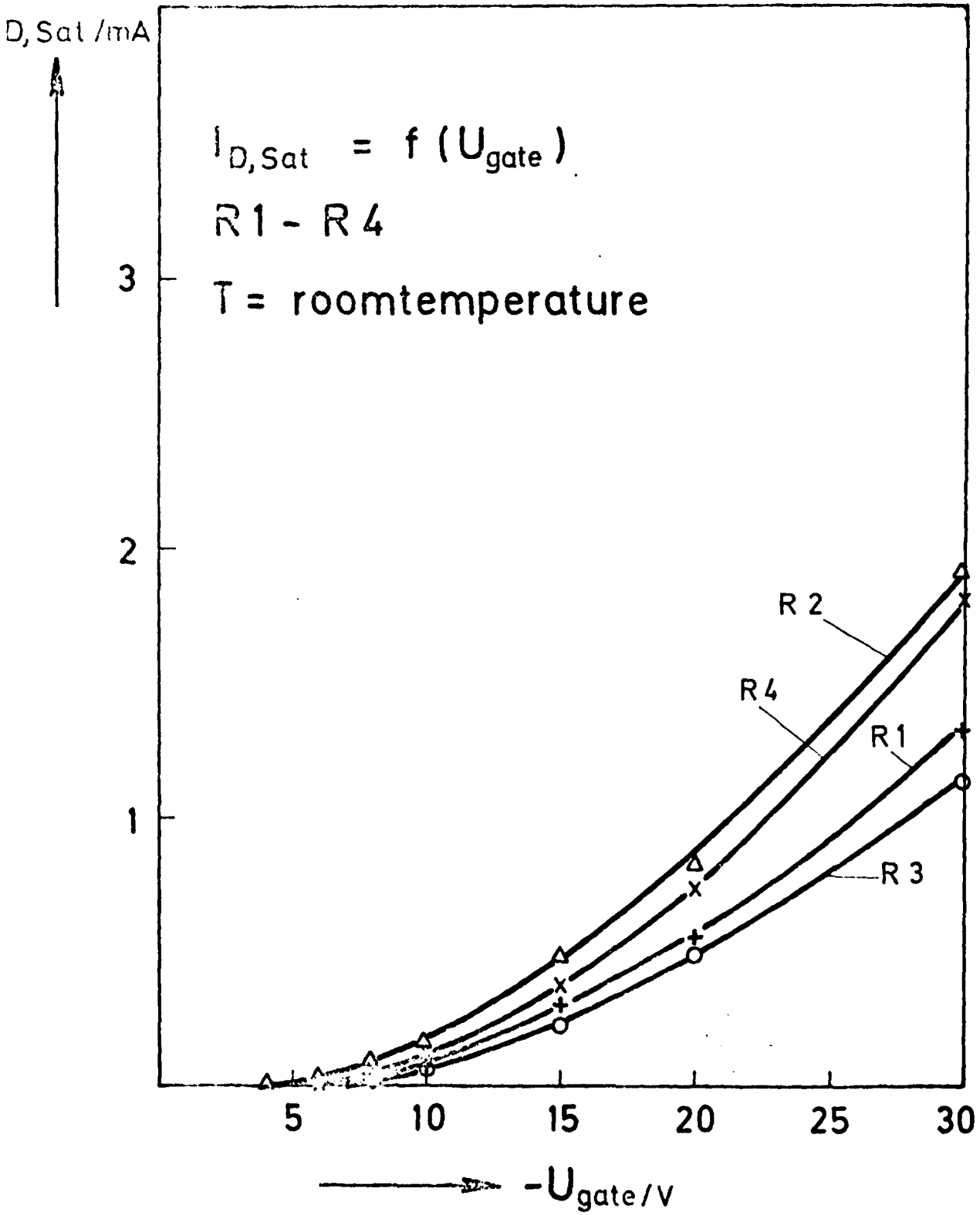
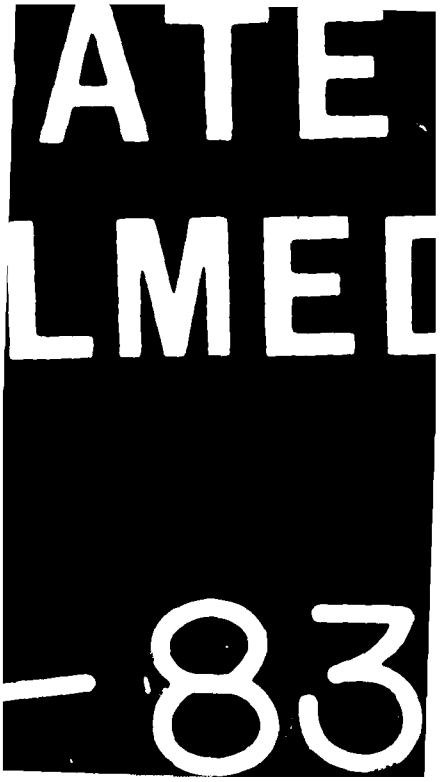

D, Sat /mA
$I_{D,Sat} = f(U_{gate})$
R 1 - R 4
T = roomtemperature
3
2
1
R 2
R 4
R 1
R 3
5
10
15
20
25
30
$-U_{gate}/V$

fig 13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